

Docket No.: MAS-FIN-410

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : RUDOLF LEHNER
Filed : CONCURRENTLY HEREWITH
Title : ELECTRONIC COMPONENT HAVING A SEMICONDUCTOR
CHIP AND METHOD FOR POPULATING A CIRCUIT CARRIER
DURING THE PRODUCTION OF THE ELECTRONIC
COMPONENT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 6,441,500 B1 (Sumikawa et al.), dated August 27, 2002;

U.S. Patent Application Publication No. 2003/0085474 A1 (Frankowsky et al.), dated May 8, 2003 and corresponding German Patent DE 101 45 468 C1 (Frankowsky et al.), dated January 16, 2003;

German Published Non-Prosecuted Patent Application DE 198 22 512 A1 (Tutsch et al.), dated October 21, 1999 and English abstract thereof;

European Patent Application EP 0 962 960 A2 (Dudderar et al.), dated December 8, 1999 and corresponding U.S. Patent No. 6,205,745 B1 (Dudderar et al.), dated March 27, 2001 and corresponding U.S. Patent No. 5,966,903 (Dudderar et al.), dated October 19, 1999;

European Patent Application EP 1 032 030 A2 (Degani et al.), dated August 30, 2000;

PCT WO 96/37913 (Tsukagoshi et al.), dated November 28, 1996 and corresponding U.S. Patent No. 5,804,882 (Tsukagoshi et al.), dated September 8, 1998;

Patent and Abstract of Japan 57031148 A (Haruo), dated February 19, 1982;

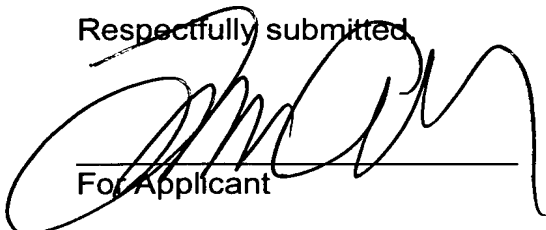
Patent and Abstract of Japan 2000269239 A (Katsutoshi), dated September 29, 2000;

Patent and Abstract of Japan 03046242 A (Koji et al.), dated February 27, 1991;

Theuß, H. et al.: "Mounting Process for Semiconductor Dice", Siemens Technik Report, 2001, pp. 1-2.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant. As per the Notice in 1273 OG 55 (August 5, 2003) no copies of any above-mentioned U.S. patents and U.S. patent application publications are submitted for any application filed after June 30, 2003.

Respectfully submitted,



For Applicant

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Date: October 30, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: MAS-FIN-410 Appl. No.: <hr/> Applicant: RUDOLF LEHNER <hr/> Filing Date: October 30, 2003 Group Art Unit:			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	6,441,500 B1	8/27/02	Sumikawa et al.			
	B	2003/0085474 A1	5/8/03	Frankowsky et al.			
	C	6,205,745 B1	3/27/01	Dudderar et al.			
	D	5,966,903	10/19/99	Dudderar et al.			
	E	5,804,882	9/8/98	Tsukagoshi et al.			
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	101 45 468 C1	1/16/03	Germany			
	K	198 22 512 A1	10/21/99	Germany			
	L	0 962 960 A2	12/8/99	Europe			
	M	1 032 030 A2	8/30/00	Europe			
	N	96/37913	11/28/96	WIPO			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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	A						
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	C						
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FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	57031148 A	2/19/82	Japan			
	K	2000269239 A	9/29/00	Japan			
	L	03046242 A	2/27/91	Japan			
	M						
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
		Theuß, H. et al.: "Mounting Process for Semiconductor Dice", Siemens Technik Report, 2001, pp. 1-2					
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